Ronald Mraz Ph.D.

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**Statement of Research**

My research interests include High Performance Computing (HPC) Architectures (Distributed Systems, Shared Memory Architectures), Message Passing Interfaces and HPC Computational Science, Operating System Interference of HPC, Control Theory, and Cybersecurity/Information Assurance.

Most recently, I have applied for support through DOD Grants for Institutional Capacity Building to provide equipment for an Experimental Cyber-Physical Lab. This would be Phase I of a multi-phase program leading to systems that will be replicated for student projects, cyber systems research, independent study and systems for lab work within the Electrical Engineering and Cyber Systems curriculum.

My current undergraduate research effort is supervision of undergraduate research in AI Image Processing for US Coast Guard related applications. A paper summarizing and categorizing all recently completed AI imaging projects in the Coast Guard. This paper is currently seeking publication submission approval to a relevant workshop or conference.

Additionally, I hosted a number of graduate student interns and visiting faculty during my tenure at IBM. My efforts were in planning their projects and mentoring the students to make the experience both intellectually stimulating and productive. In many cases their work lead to publications of following on job offers or continued research.

As a new tenure track professional, I would be excited to participate in the current research in computational science that is currently funded. Additionally, I would look to submit an NSF CAREER multi-year proposal for research in one of the following fields I have identified.

In my current position, I have developed a working relationship with the Coast Guard Research and Development Center. This will allow me to prepare proposals in relevant areas of research for funding in the areas of Imagery and HPC. Additionally, I have a number of contacts at Industry and US National Labs that will help in proposing areas of research in HPC, Information Security and Computer Organization.

Finally, my extensive experience in writing both domestic and international patents that have issued can facilitate royalty income for USC and the inventors from innovations conceived by the department.

Included here are short descriptions of the work done in my years of industrial research with selected publications*.*

**Message Passing Interfaces and HPC Computational Science**

My research includes the writing several message-passing libraries for High Performance Computing (HPC) shared and distributed memory systems. These messages passing systems were validated with established benchmarks for molecular dynamics modelling, automobile crash simulations, FFT for oil exploration, weather modelling and an enhanced database system (IBM DB2) for parallel operation on HPC systems. Additionally, I modeled induction motor designs in computer simulations to optimize feedback parameters for digital controls. Furthermore, I would like to apply this work to the emerging area of Computational Science.

Having done original work on video over ATM, enabled by a custom high-performance interface, described in “A high performance Get-Put interface for ATM communications”. This effort was further used by researchers for message passing interfaces analysis.

*“A high performance Get-Put interface for ATM communications”,* **In Proceedings of the** **Centre for Advanced Studies Conference (CASCON),** 1998.

 *“EUIm: A message passing library for the IBM power visualization system,”* in **Proceedings of the IEEE Workshop on Advances in Parallel and Distributed Systems**, 1993, Pages: 53 – 58. (IDA Gov’t Contract)

**Cybersecurity/Information Assurance**

I provided the technical direction of Owl Computing Technologies, Inc. which sold special purpose internet firewalls with the security policies enforced by a hybrid HW/SW system. The company was started from licensing a concept patent (US Patent5,703,562) from Sandia National Labs. In doing so, pioneered the data-diode security market by evolving the technology to a scalable appliance for cyber security. The technology used in all products is certified by the National Information Assurance Partnership (NIAP).

The security industry has a number of emerging technologies that require research and development for commodity use. One technology is Secure Linux where an application’s operations and interactions with the system are confined by a set of rules. These is currently research in confining the operating system executables, which will significantly harden computing systems. This and other technologies, such as blockchains, are opening new areas of research and product opportunities.

Earlier in my career, I had researched optimizing SSL communications for scalability at IBM. Patents assigned to Owl Computing and IBM make up my 51 issued patents in the US.

Curt Nilsen, *“Method for transferring data from an unsecured computer to a secured computer”* **US Patent****5,703,562,** Issued December 30, 1997 (Licensed from Sandia in 1999)

*“Performance Considerations in Web Security*,” **Chapter in Certification and Security in E-Services. IFIP – The International Federation for Information Processing**, vol 127. 2002, Pages 57-71, Springer, Boston, MA.

*“Using SSL Session ID Reuse for Characterization of Scalable Secure Web Servers”,* **Technical Report RC 22323(Revised May 5, 2002),** IBM Research Division, Yorktown Heights, NY, September 2002.

 *“Secure Blue: an architecture for a scalable, reliable high-volume SSL Internet server,”* in the **Annual Computer Security Applications Conference (ACSAC)** Year: 2001, New Orleans, Louisiana, 2001.

*“Fact extraction from bash in support of script migration,”* in Software Evolution Week - **IEEE Conference on Software Maintenance, Reengineering, and Reverse Engineering** (CSMR-WCRE), 2014, Pages: 363 – 366. (Owl funded research at Univ. of Waterloo)

“Secure Cross Border Information Sharing Using One-Way Data Transfer Systems”, Presented at **ISGIG, the International Symposium on Global Information Governance** in Pisa, Italy. 2009.

 *“Coalition Warrior Interoperability Demo (CWID) 2007 Data Diode Case Study”,* Invited **Annual Computer Security Applications Conference (ACSAC),** 2007 Presentation.

*“Transferring Large files in Real-Time”,* Presented at the **2nd Int’l Workshop on Operating System Interference in High Performance Applications (OSIHPA),** 2006. In conjunction with PACT-06.

**Operating System Interference of HPC**

I have done several investigations into operating system interference of HPC systems. At the forefront is the work of characterizing the extent that operating systems impede the scalability of parallel program execution. I have also co-organized workshops on operating system interference. As commodity networks improve in both latency and bandwidth, it is imperative that the features added in commodity operating systems do not impede the scalability of HPC systems.

The work on "Reducing the variance of point-to-point transfers for parallel real-time programs," was based on measuring latencies among a set of processors using a simple “hot potato” messaging application (each processor received a single message (the “potato”) and immediately passed it to the next in a list. This approach revealed the degree to which background operating system activities and other interrupts may impacted the variance of tasks with real-time constraints, and showed a path to a possible solution.

*"Reducing the variance of point-to-point transfers for parallel real-time programs*," in IEEE Parallel & Distributed Technology: Systems & Applications, vol. 2, no. 4, pp. 20-31, Winter 1994.

*“Reducing the variance of point to point transfers in the IBM 9076 parallel computer, “in* **Supercomputing '94: Proceedings of the 1994 ACM/IEEE Conference on Supercomputing**, 1994, Pages: 620 – 629.

*“*The Effect of Operating System Scheduling on High Performance Message Passing Parallel Systems*”* in **Proceedings of the 7th Intl. Conference on Parallel and Distributed Computing Systems (PDCS ’94)**  Las Vegas, Nevada 1994, Pages: 100 – 104. (IDA Gov’t Contract)

**Real-Time Systems**

My Ph.D thesis developed the design of a pipelined RISC processor that supports dynamic scheduling of real-time applications with little or no noticeable overhead. The processor design subsumes scheduling overhead through the concurrent execution of an Embedded Scheduler. The idea employed an embedded scheduler within the stall cycles of existing applications. The simulations show that the concept can improve system utilization by as much as 28 percent offering a potential performance gain of 40 percent over traditional timer driven scheduling techniques.

R. Mraz, **Ph.D., Electrical and Computer Engineering, Carnegie Mellon University 1992.** Pittsburgh, PA. Thesis topic: “*A RISC-Based Architecture for Real-Time Computation”*. Thesis Committee: Jay K. Strosnider, John P. Shen, Zary Segall and Gabriel Silberman.

Available at <https://www.ece.cmu.edu/research/publications/1992/CMU-ECE-1992-070.pdf>

*“A methodology to evaluate architectures for real-time control,”* in the **IEEE International Conference on Systems Engineering,** 1990 Pages: 449 - 453,

*“Analysis of architectures for fault-tolerant computation,”* in the Proceedings of the **IEEE** **Twenty-Fourth Annual Hawaii International Conference on System Sciences**, Year: 1991, Pages: 334 - 343 vol.1.

*“A methodology to evaluate architectures for real-time control,”* in the **IEEE International Conference on Systems Engineering,** 1990 Pages: 449 - 453,

**High Performance Computing Architectures**

Early in my career, I was tasked with redesigning the Cray Architecture in IBM technology. Later, I participated in several supercomputer prototype designs in both shared memory and distributed memory architectures. What had taken an entire room of computers back then can now be done in a single server with multiple cores. Having such computing cores linked with shared memory offers a new realm of possibilities. Revamping my HPC scalability research with these powerful shared memory environments is an interesting area of research to extend my prior work.

Later, I had participated in research of TCP offload organization, I/O enhancements using the paging hardware for a-priori zero copy movement of data from IO devices to main memory as well as fault tolerance analysis of general purpose computer organizations.

*“Server Network Scalability and TCP Offload*,” in **USENIX Annual Technical Conference,** 2005, Pages 209 – 222.

*“A study of virtual memory MTU reassembly within the PowerPC architecture*,” in **Proceedings of the IEEE Fifth International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems (MASCOTS),** 1997, Pages: 81 – 90.

Sincerely,

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